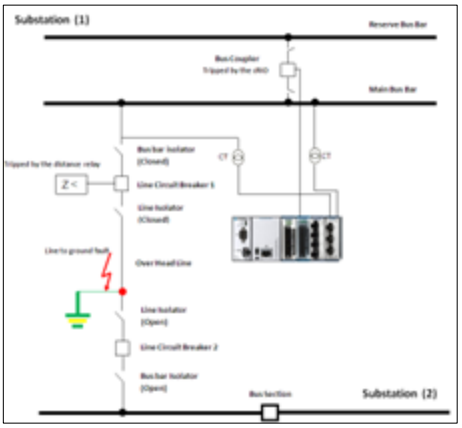
Client : National Electric Power Company.
Project: NEPCO Digital Fault Protection System.



NEPCO opted to work with Technology Integration on this project for the programmability and customizability of the system. NI's cRIO platform is programmed in LabVIEW across both the FPGA platform, and the real-time controller.

System Description:

The system consists of four electrical current signals, circuit breaker trip signal, GPS signal and GSM signal.

Software:

The software of this application was developed to monitor trip and record the short circuit currents in a bus coupler.

Description:

The main purpose of the system is to protect the power system when two parallel bus bars are connected through a bus coupler. When the bus coupler is closed for load transfers, the value of the short circuit currents flowing in the line will increase and might double. It may increase up to a limit which may come close to the rated current of the line circuit breaker; it may also cause damages to the bus bars and the line circuits. If the fault current is not interrupted when the bus bars are coupled, this may cause power outage within the coupled bus bars.

Lowering the short circuit fault current was achieved by opening the bus coupler in less than 1ms, thus decreasing the coupled bus bar contribution to the fault current in the line, allowing the line circuit breaker to open at a lower fault current.

In this case, the cRIO was used as a relay that sent a trip signal to the bus-coupler if two conditions met: the current and the current time derivative exceed the pre-set limits. The current time derivative is calculated to differentiate between fault currents and in-rush currents of inductive loads

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Figure 1 shows a plot of the fault current flowing in the over head line and the fault current flowing in the bus coupler from the time of fault initiation till the fault was cleared. As can be seen, the bus coupler's fault current was brought to zero allowing the line circuit breaker to open on a lower value of fault current.

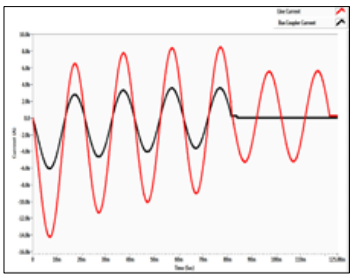
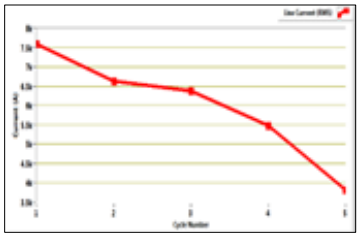


Figure 2 displays the RMS Line current measured each cycle, it shows how the line current is being reduced due to the decoupling of the bus bars.
Advantages:



- Ultra rapid response of 20 microseconds;
- Deterministic operation using a Real Time OS and FPGA; Protecting other substations on the network that can be affected by the fault;
- Fault waveform logging and display with digital inputs from the circuit breakers;
- Configurable alarms; Easy to log and retrieve Data; Expandable I/O modules.